

## 1. Product profile

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### 1.1 General description

A 500 W to 600 W LDMOS power transistor for broadcast applications and industrial applications in the HF to 500 MHz band.

Table 1. Application information

Mode of operation	f	V <sub>DS</sub>	P <sub>L</sub>	G <sub>p</sub>	η <sub>D</sub>
	(MHz)	(V)	(W)	(dB)	(%)
CW	225	50	500	26.5	70
	108	50	600	27.5	73

### 1.2 Features and benefits

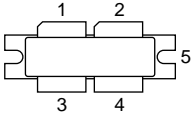
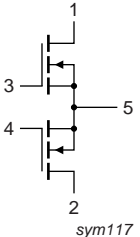
- Typical CW performance at frequency of 225 MHz, a supply voltage of 50 V and an I<sub>DQ</sub> of 1000 mA:
  - ◆ Average output power = 500 W
  - ◆ Power gain = 26.5 dB
  - ◆ Efficiency = 70 %
- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (10 MHz to 500 MHz)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

### 1.3 Applications

- Industrial, scientific and medical applications
- Broadcast transmitter applications

## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1		 sym117
2	drain2		
3	gate1		
4	gate2		
5	source <sup>[1]</sup>		

[1] Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF574	-	flanged balanced LDMOST ceramic package; 2 mounting holes; 4 leads	SOT539A

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	110	V
$V_{GS}$	gate-source voltage		-0.5	+11	V
$I_D$	drain current		-	56	A
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature		-	225	°C

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}; P_L = 400\text{ W}$	0.23	K/W

[1]  $R_{th(j-c)}$  is measured under RF conditions.

## 6. Characteristics

**Table 6. DC characteristics**

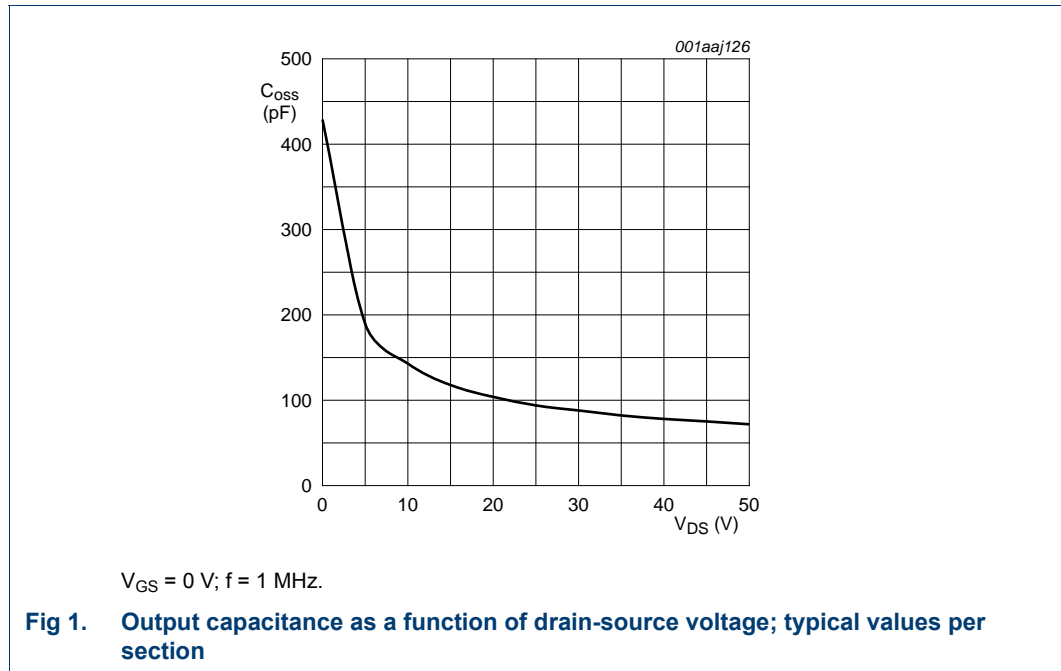
$T_j = 25\text{ }^\circ\text{C}$ ; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 2.5\text{ mA}$	110	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 250\text{ mA}$	1.25	1.7	2.25	V
$V_{GSq}$	gate-source quiescent voltage	$V_{DS} = 50\text{ V}; I_D = 500\text{ mA}$	1.35	1.85	2.35	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V}$	-	-	2.8	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	29	37.5	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	280	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 12.5\text{ A}$	-	17	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 8.33\text{ A}$	-	0.14	-	$\Omega$
$C_{rs}$	feedback capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V}; f = 1\text{ MHz}$	-	1.5	-	pF
$C_{iss}$	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V}; f = 1\text{ MHz}$	-	204	-	pF
$C_{oss}$	output capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V}; f = 1\text{ MHz}$	-	72	-	pF

**Table 7. RF characteristics**

Mode of operation: CW;  $f = 225\text{ MHz}$ ; RF performance at  $V_{DS} = 50\text{ V}; I_{Dq} = 1000\text{ mA}$  for total device;  $T_{case} = 25\text{ }^\circ\text{C}$ ; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_p$	power gain	$P_L = 400\text{ W}$	25	26.5	28	dB
$RL_{in}$	input return loss	$P_L = 400\text{ W}$	13	20	-	dB
$\eta_D$	drain efficiency	$P_L = 400\text{ W}$	66	70	-	%



### 6.1 Ruggedness in class-AB operation

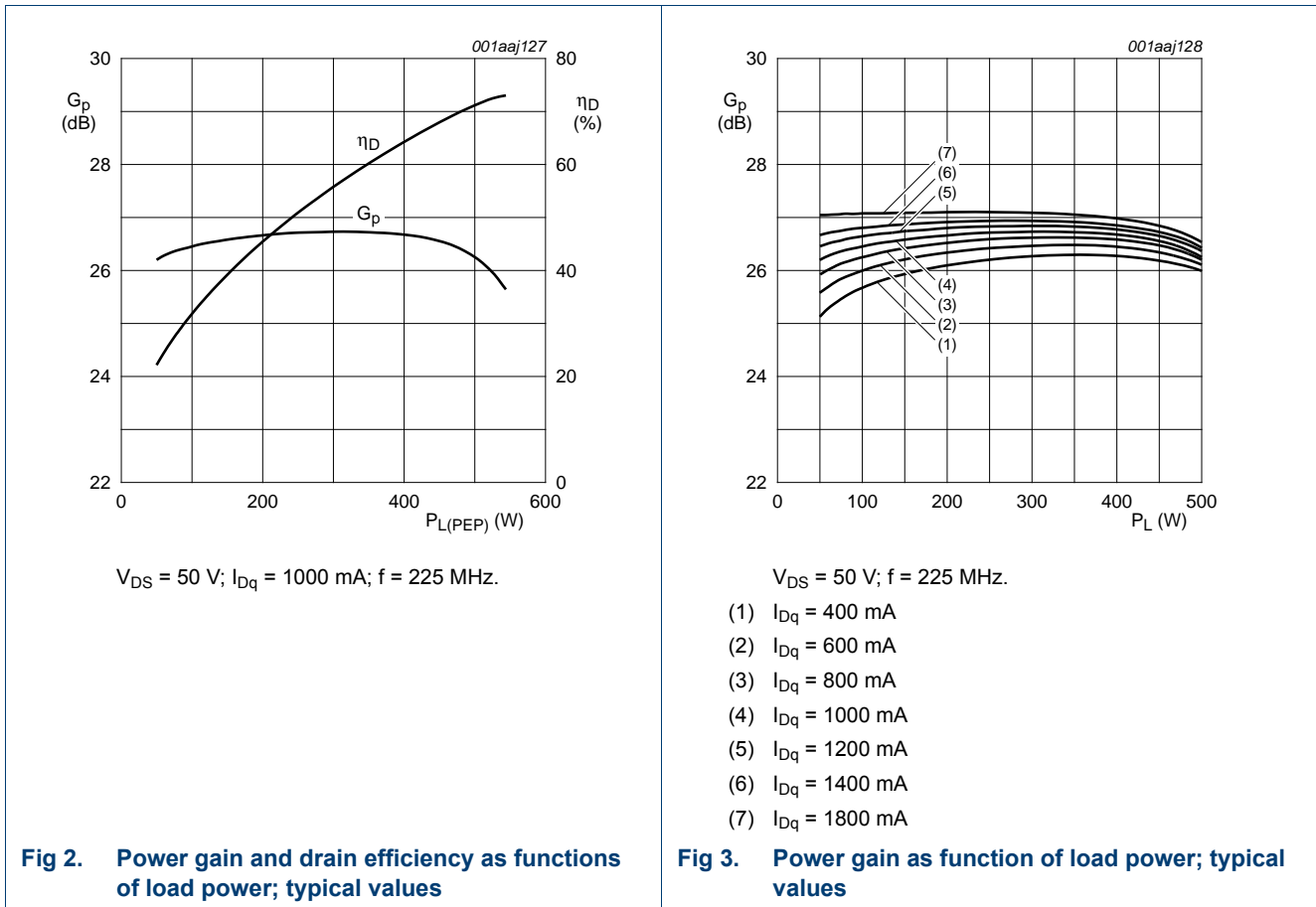
The BLF574 is capable of withstanding a load mismatch corresponding to VSWR = 13 : 1 through all phases under the following conditions:  $V_{DS} = 50 \text{ V}$ ;  $I_{Dq} = 1000 \text{ mA}$ ;  $P_L = 400 \text{ W}$ ;  $f = 225 \text{ MHz}$ .

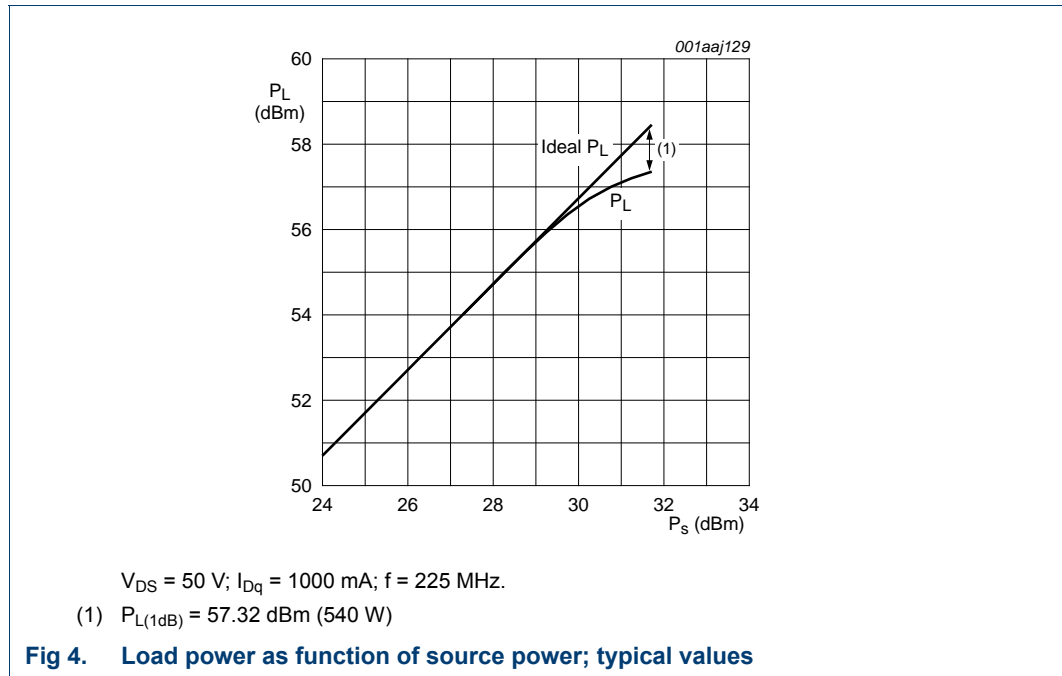
## 7. Application information

### 7.1 RF performance

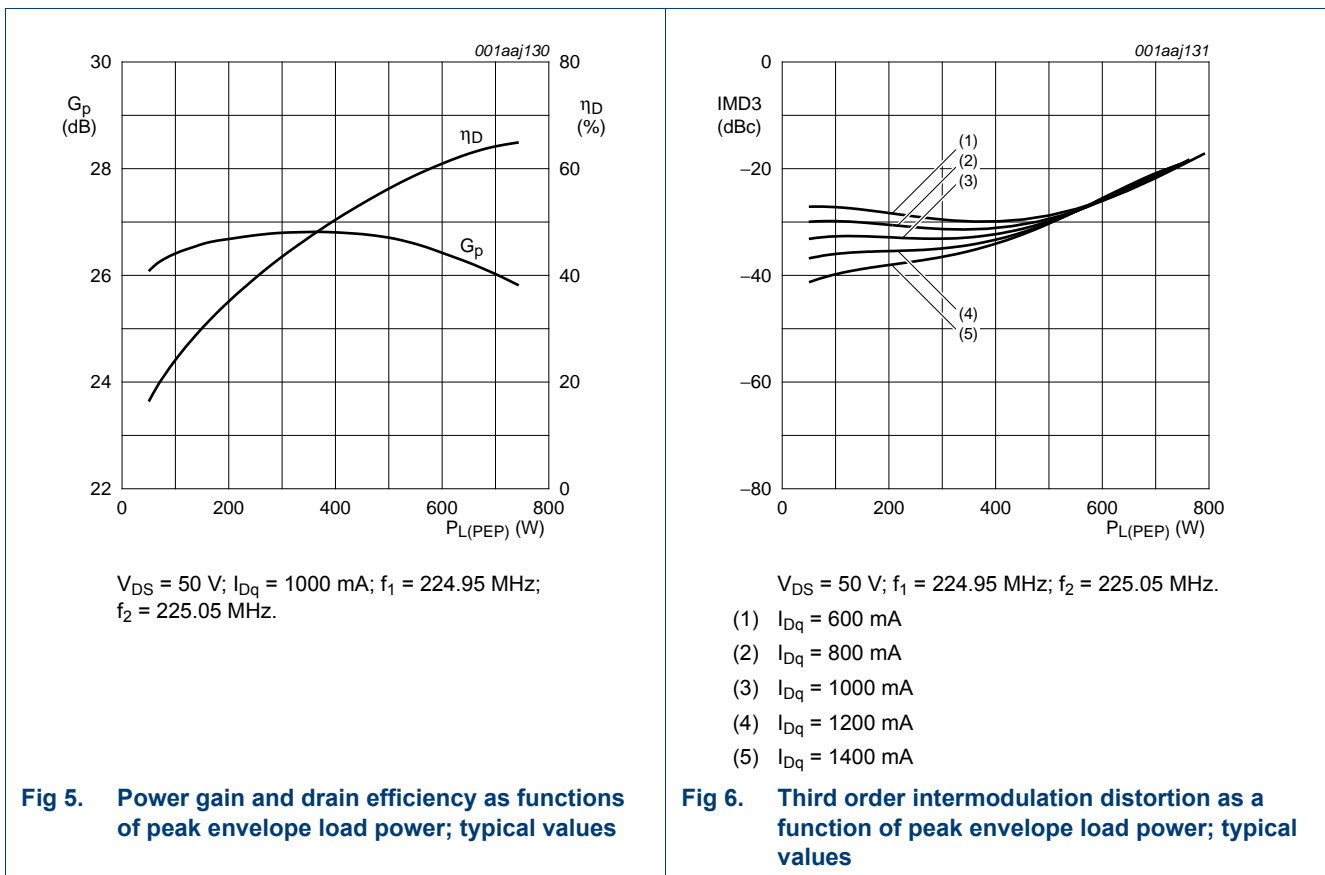
RF performance in a 500 W application circuit at 225 MHz.

#### 7.1.1 1-Tone CW





7.1.2 2-Tone CW



7.1.3 Application circuit

**Table 8. List of components**

For application circuit, see [Figure 7](#).

Printed-Circuit Board (PCB): Rogers 5880;  $\epsilon_r = 2.2$  F/m; height = 0.79 mm; Cu (top/bottom metallization); thickness copper plating = 35  $\mu$ m.

Component	Description	Value	Remarks
C1, C2, C23, C24	multilayer ceramic chip capacitor	100 pF <a href="#">[1]</a>	
C3	multilayer ceramic chip capacitor	24 pF <a href="#">[1]</a>	
C4, C5	multilayer ceramic chip capacitor	39 pF <a href="#">[1]</a>	
C6, C9	multilayer ceramic chip capacitor	4.7 $\mu$ F	TDK4532X7R1E475Mt020U
C7, C8, C10, C11	multilayer ceramic chip capacitor	1 nF <a href="#">[1]</a>	
C12, C16	electrolytic capacitor	220 $\mu$ F; 63 V	
C13, C15	multilayer ceramic chip capacitor	62 pF <a href="#">[1]</a>	
C14	multilayer ceramic chip capacitor	15 pF <a href="#">[1]</a>	
C17, C19	multilayer ceramic chip capacitor	47 pF <a href="#">[1]</a>	
C18	multilayer ceramic chip capacitor	33 pF <a href="#">[1]</a>	
C20, C22	multilayer ceramic chip capacitor	10 pF <a href="#">[1]</a>	
C21	multilayer ceramic chip capacitor	18 pF <a href="#">[1]</a>	
L1, L2, L3, L4	3 turns 1 mm copper wire	D = 3 mm; length = 3 mm	
L5, L6	stripline	-	(L x W) 125 mm x 7 mm
L7, L8, L9, L10	stripline	-	(L x W) 8 mm x 15 mm
L11, L12	stripline	-	(L x W) 132 mm x 7 mm
R1, R2	metal film resistor	10 $\Omega$ ; 0.6 W	
R3, R4	metal film resistor	3 $\Omega$ ; 0.6 W	
T1, T2, T3, T4	semi rigid coax	50 $\Omega$ ; 120 mm	EZ-141-AL-TP-M17

[1] American Technical Ceramics type 100B or capacitor of same quality.

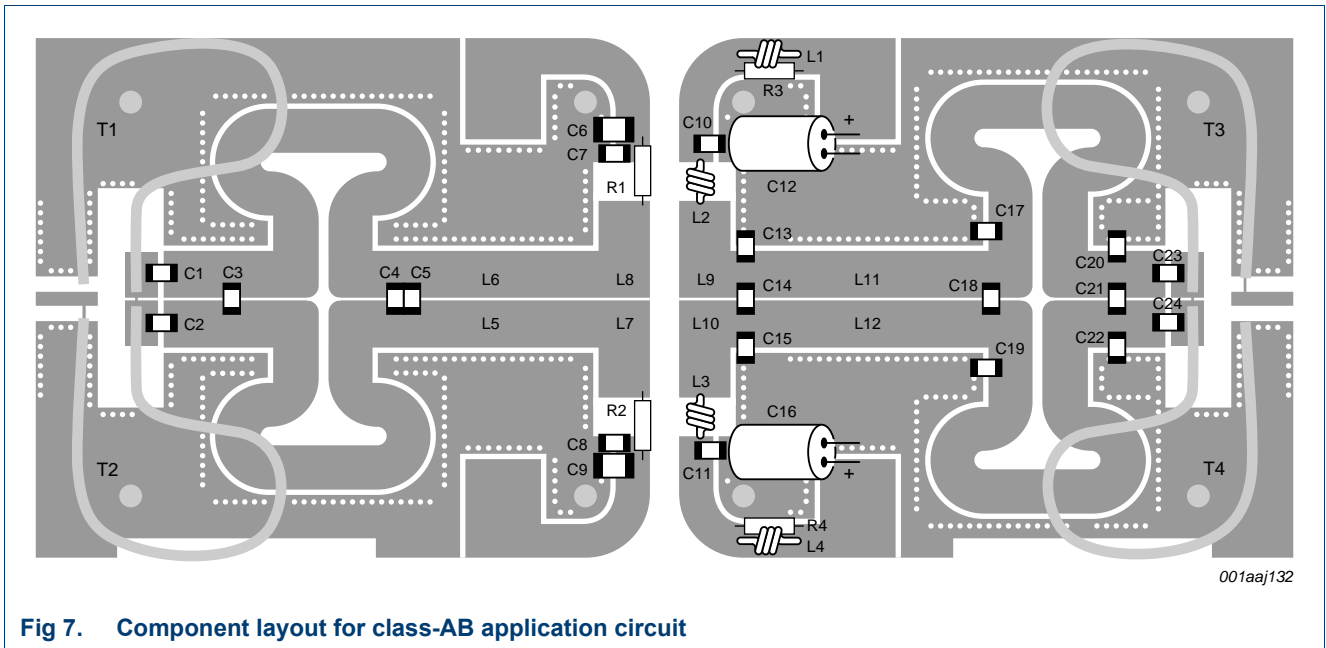
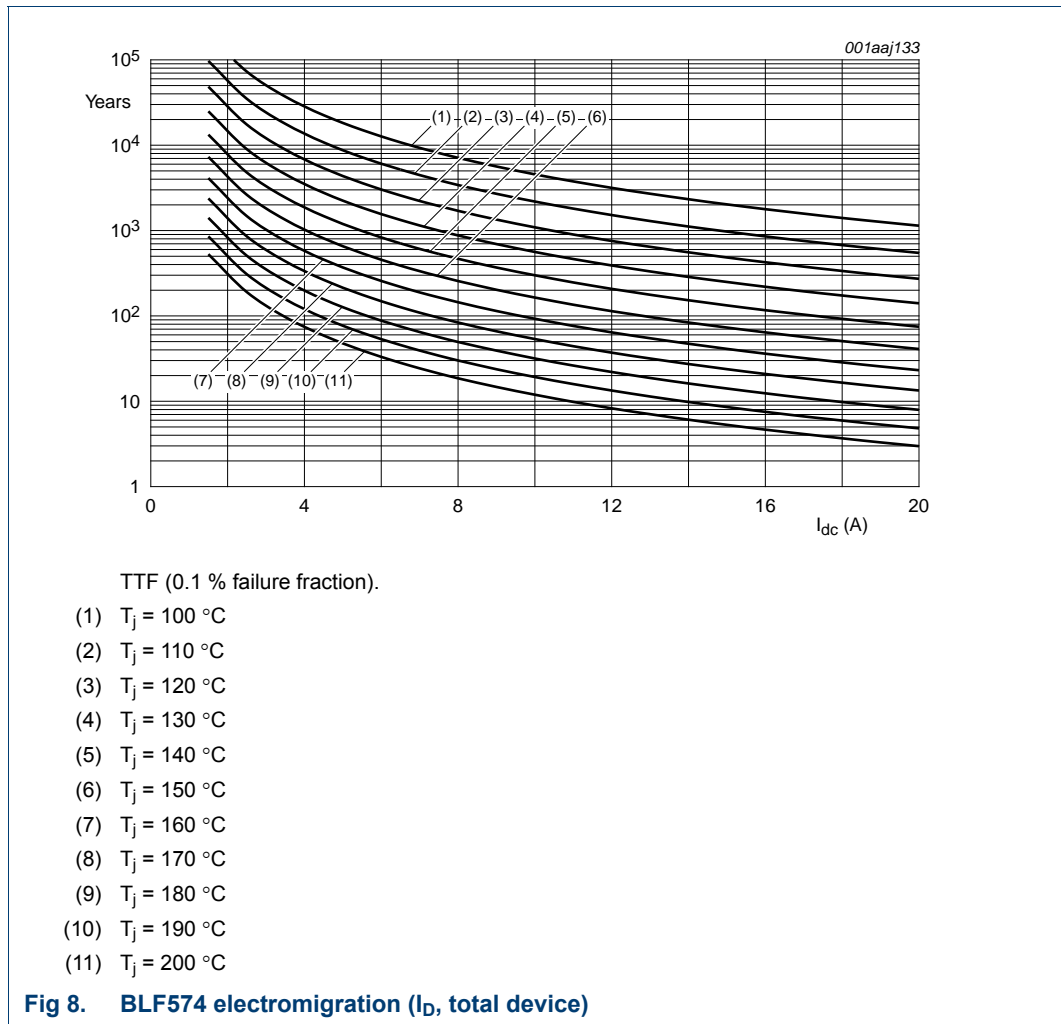


Fig 7. Component layout for class-AB application circuit



7.2 Reliability

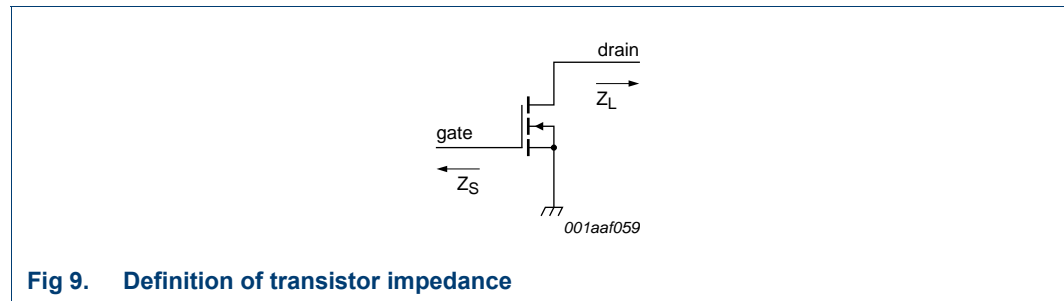


## 8. Test information

### 8.1 Impedance information

**Table 9. Typical impedance**  
 Simulated  $Z_S$  and  $Z_L$  test circuit impedances.

f	$Z_S$	$Z_L$
MHz	$\Omega$	$\Omega$
225	$3.2 + j2.5$	$7.5 + j4.0$

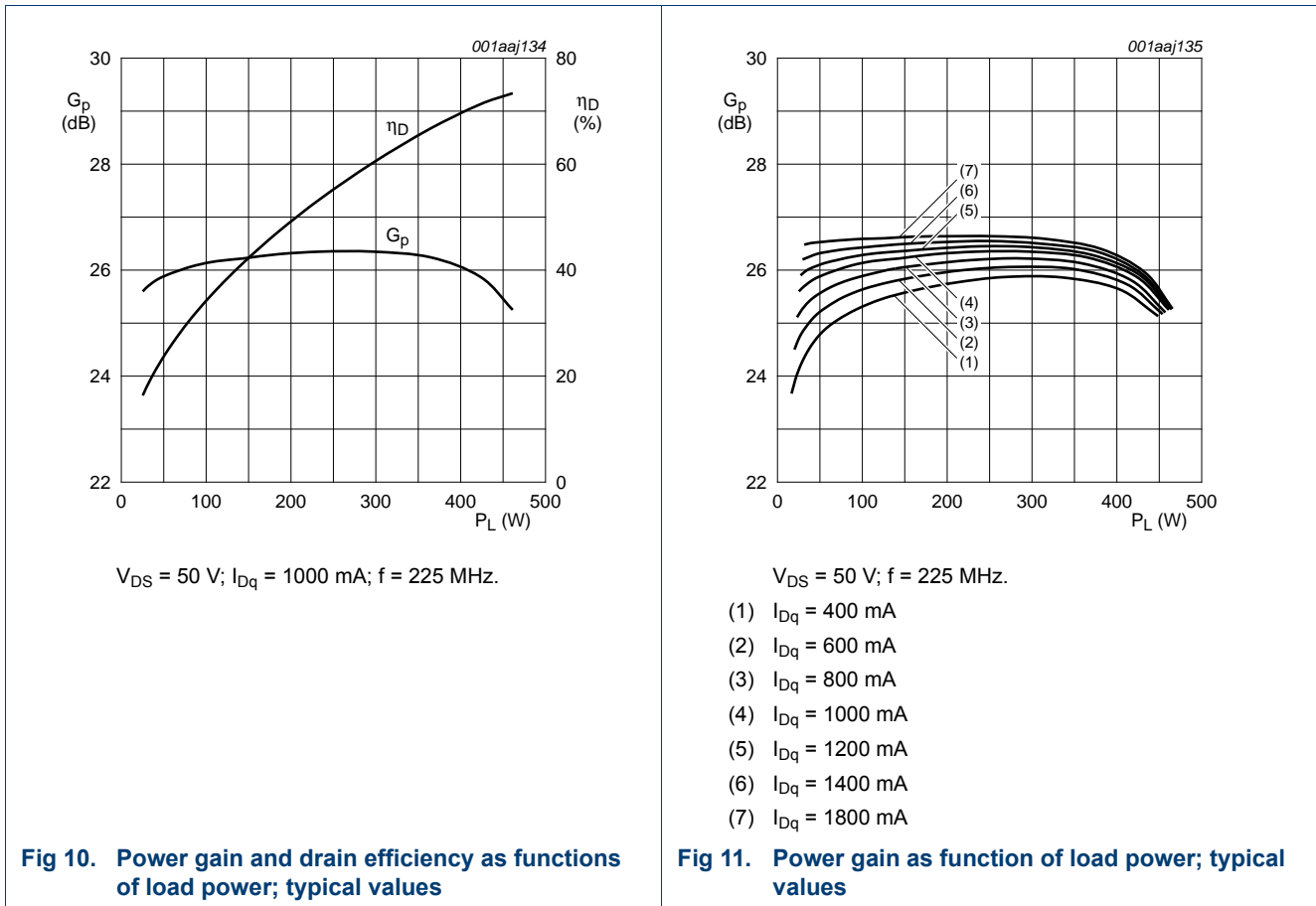


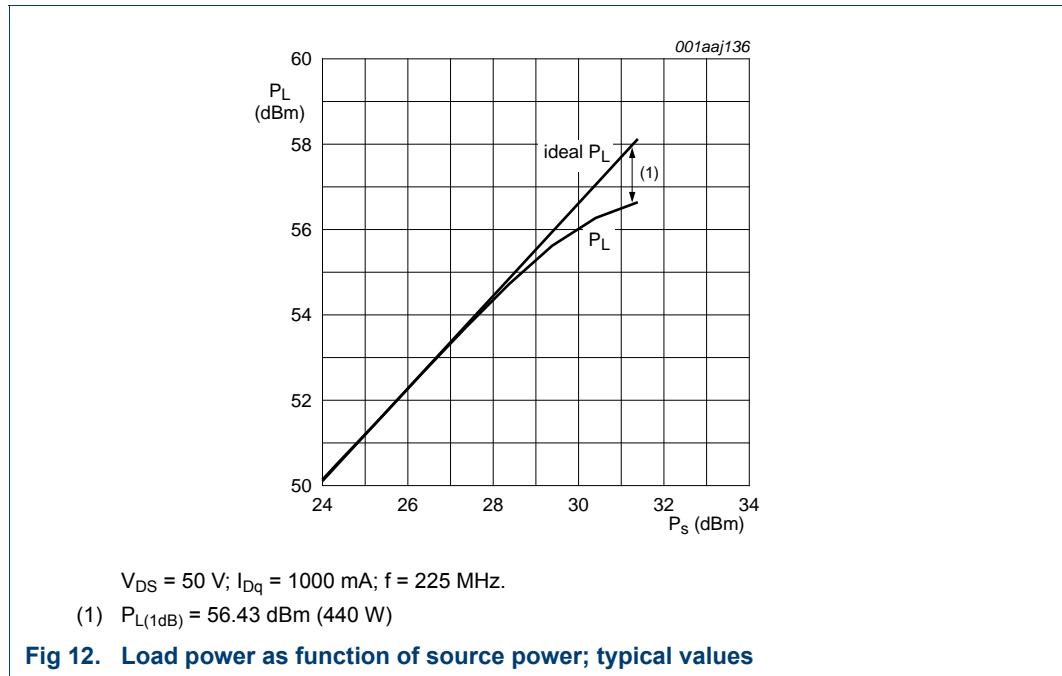
**Fig 9. Definition of transistor impedance**

## 8.2 RF performance

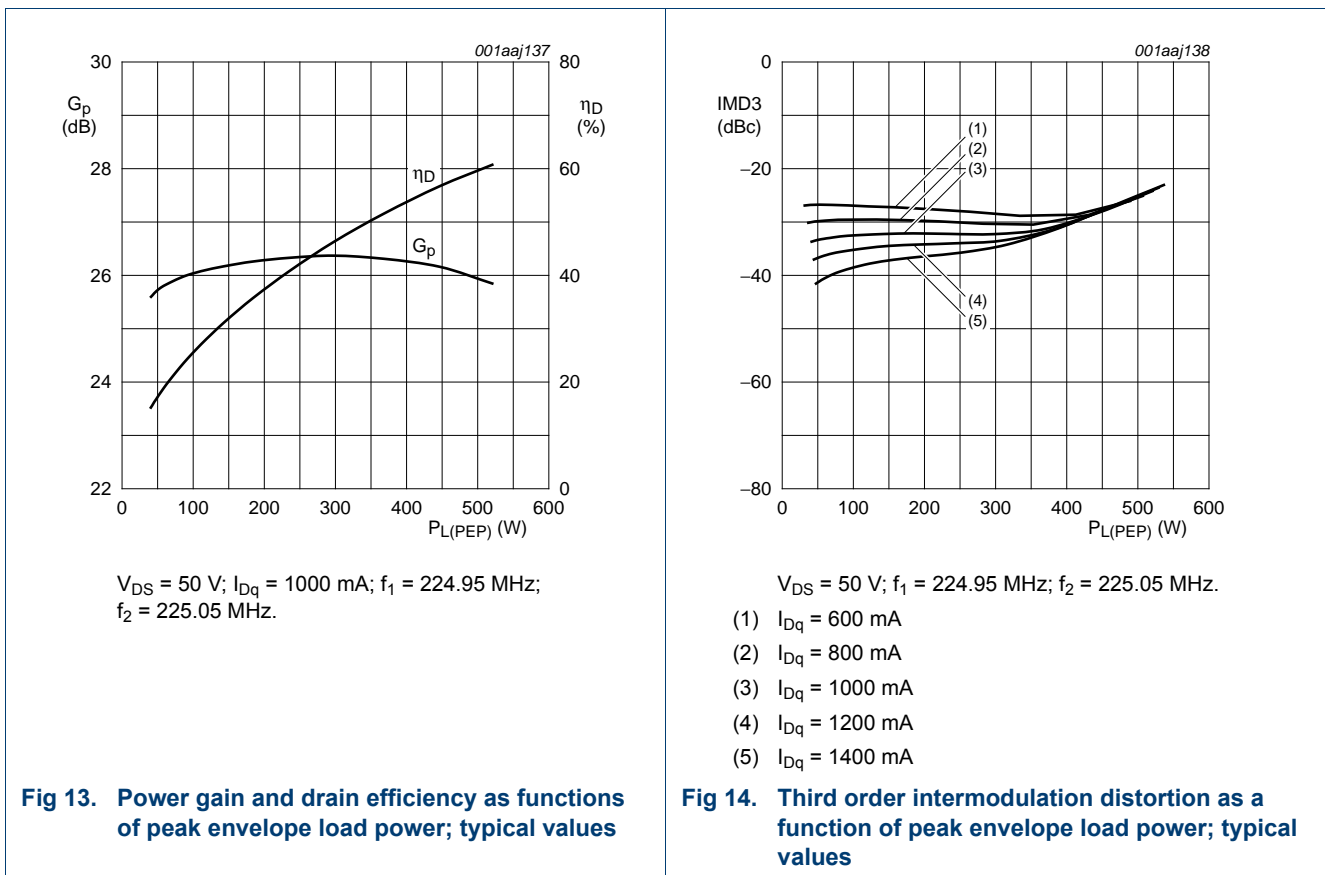
The following figures are measured in a class-AB production test circuit.

### 8.2.1 1-Tone CW





8.2.2 2-Tone CW



### 8.2.3 Test circuit

**Table 10. List of components**

For production test circuit, see [Figure 15](#) and [Figure 16](#).

Printed-Circuit Board (PCB): Rogers 5880;  $\epsilon_r = 2.2$  F/m; height = 0.79 mm; Cu (top/bottom metallization); thickness copper plating = 35  $\mu\text{m}$ .

Component	Description	Value	Remarks
C1, C2, C20, C21	multilayer ceramic chip capacitor	100 pF <a href="#">[1]</a>	
C3	multilayer ceramic chip capacitor	24 pF <a href="#">[1]</a>	
C4, C5	multilayer ceramic chip capacitor	39 pF <a href="#">[1]</a>	
C6, C7, C10, C11	multilayer ceramic chip capacitor	1 nF <a href="#">[1]</a>	
C8, C9	multilayer ceramic chip capacitor	4.7 $\mu\text{F}$ <a href="#">[1]</a>	TDK4532X7R1E475Mt020U
C12, C13	electrolytic capacitor	220 $\mu\text{F}$ ; 63 V	
C14, C15	multilayer ceramic chip capacitor	47 pF <a href="#">[1]</a>	
C16	multilayer ceramic chip capacitor	33 pF <a href="#">[1]</a>	
C17	multilayer ceramic chip capacitor	18 pF <a href="#">[1]</a>	
C18, C19	multilayer ceramic chip capacitor	10 pF <a href="#">[1]</a>	
C22	multilayer ceramic chip capacitor	15 pF <a href="#">[1]</a>	
C23, C24	multilayer ceramic chip capacitor	62 pF <a href="#">[1]</a>	
L1, L2, L3, L4	3 turns 1 mm copper wire	D = 3 mm; length = 2 mm	
L5, L6	stripline	-	(L x W) 125 mm x 7 mm
L7, L8, L9, L10	stripline	-	(L x W) 8 mm x 15 mm
L11, L12	stripline	-	(L x W) 132 mm x 7 mm
R1, R2	metal film resistor	10 $\Omega$ ; 0.6 W	
R3, R4	metal film resistor	3 $\Omega$ ; 0.6 W	
T1, T2, T3, T4	semi rigid coax	50 $\Omega$ ; 120 mm	EZ-141-AL-TP-M17

[1] American Technical Ceramics type 100B or capacitor of same quality.

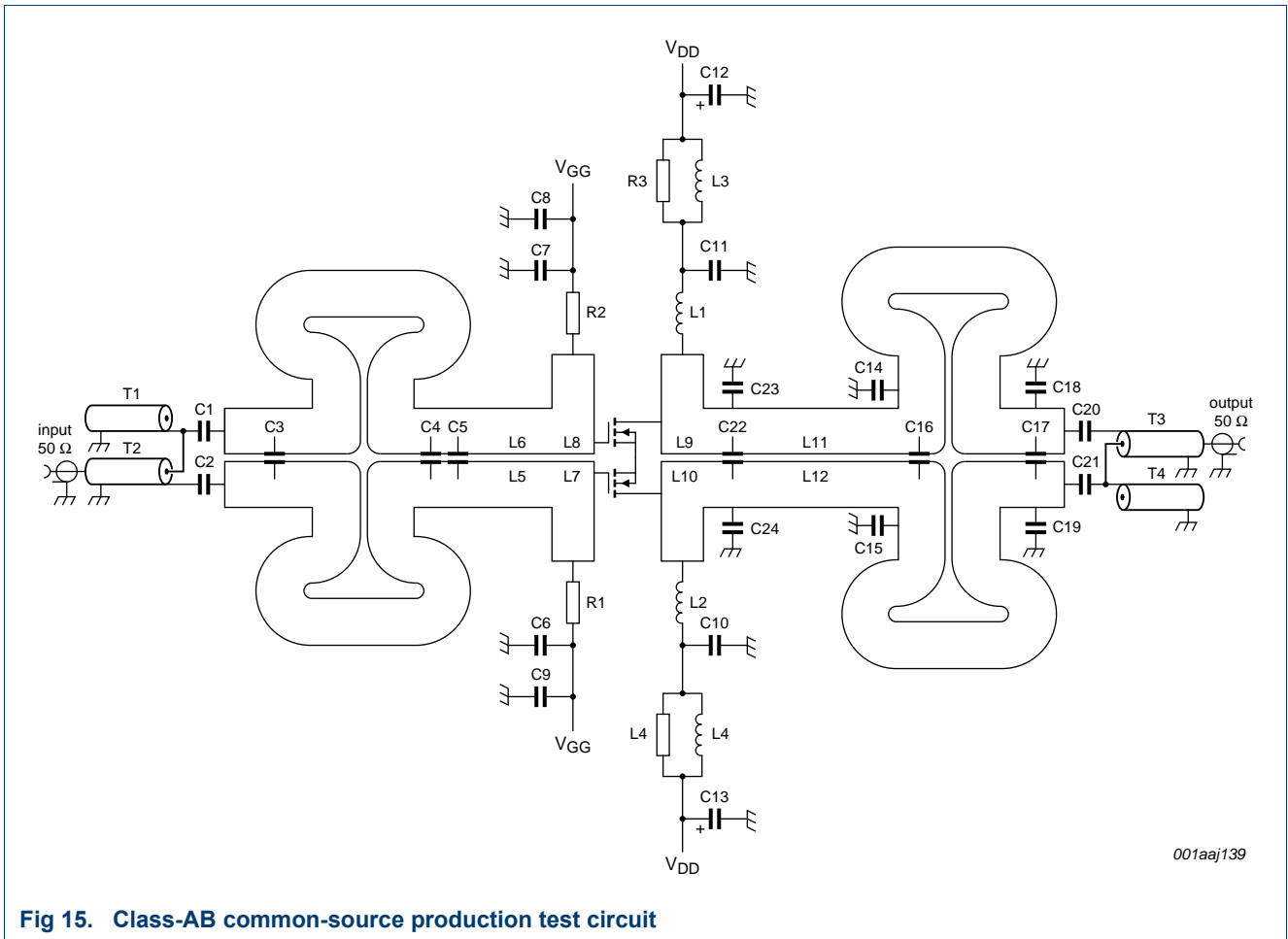


Fig 15. Class-AB common-source production test circuit

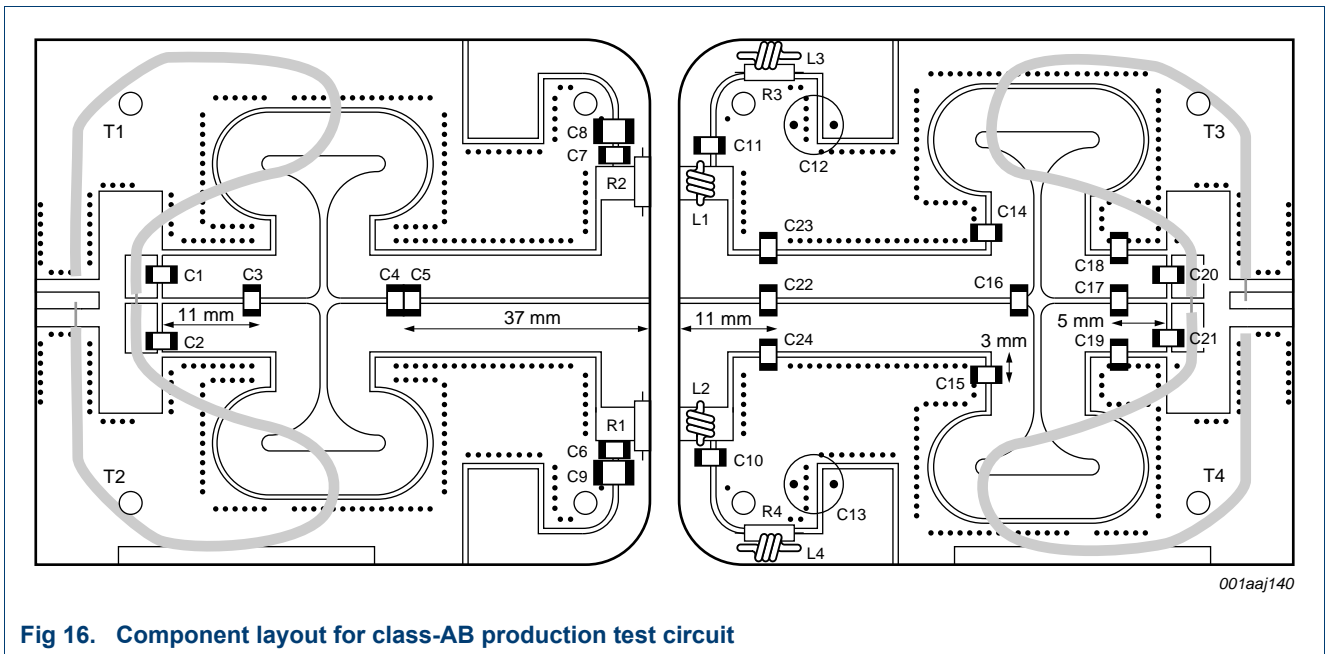


Fig 16. Component layout for class-AB production test circuit

9. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads

SOT539A

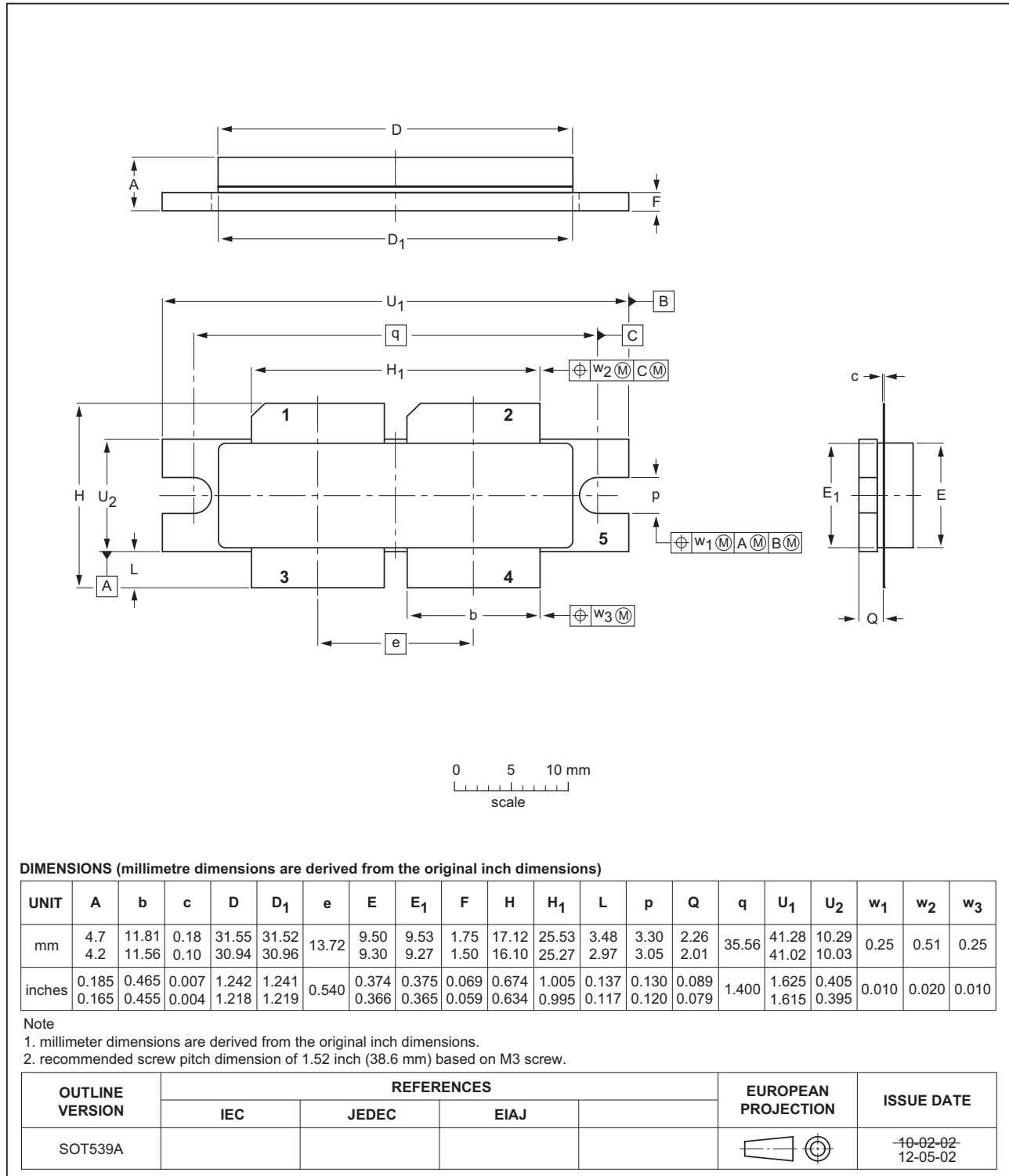


Fig 17. Package outline SOT539A

## 10. Handling information

### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 11. ESD sensitivity

ESD model	Class
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 <a href="#">[1]</a>

[1] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V, but fails after exposure to an ESD pulse of 4000 V.

## 11. Abbreviations

Table 12. Abbreviations

Acronym	Description
CW	Continuous Wave
EDGE	Enhanced Data rates for GSM Evolution
GSM	Global System for Mobile communications
HF	High Frequency
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
RF	Radio Frequency
TTF	Time To Failure
VHF	Very High Frequency
VSWR	Voltage Standing-Wave Ratio

## 12. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF574 v.4	20161201	Product data sheet	-	BLF574_3
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 10 on page 16</a>: updated Handling information</li> </ul>			
BLF574_3	20150901	Product data sheet	-	BLF574_2
BLF574_2	20090224	Product data sheet	-	BLF574_1
BLF574_1	20081208	Preliminary data sheet	-	-



## 13. Legal information

### 13.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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